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geiger

Geiger TRNG emitter: the detector and an ESP32-C6 in a box

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# Geiger TRNG emitter: the detector and an ESP32-C6 in a box

The Pi 4 bench retired 2026-10-05 after its USB-C power plug melted. What replaces it: the CAJOE board and an opto in a box, an ESP32-C6 board beside them that does one thing (latch the time of each count in hardware at 6.25 ns and send it), and every bit of processing on a server. The plan in words is docs/HARDEN-PLAN.md.

COUNTING SINCE 2026-10-10. No opto on P3 could ever light: its INT pin hangs off Q3's collector through R19 (470k) and passes 5 uA. The tap as built is a wire on R19's collector end, and sheet 3 now draws it. Each count makes about two falling edges (issue 5); the extractor holds off 2 ms, and behind that dead time the counts are Poisson ( $p = 0.59$  on 41,332 intervals). Firmware emitter-0.2. Since 2026-10-11 the detector and the opto are sealed in an outdoor container inside a metal chassis, in a garage out of the sun; the emitter is outside it on a USB brick and the CAJOE is alone on the chassis supply's 5 V line (owner, 2026-10-13): 10.65 counts a second, Wi-Fi at -50 dBm from outside the metal. Nothing on these sheets is marked not confirmed now; the chassis's bond to ground is the one thing not read.

## Sheets

| SHEET | TITLE                                                  | PAPER  | HOW IT IS MADE           |
|-------|--------------------------------------------------------|--------|--------------------------|
| 1     | Cover and sheet index                                  | letter | this sheet               |
| 2     | System: what crosses each boundary                     | ANSI B | schematic                |
| 3     | The box: the CAJOE on 5 V, the opto on Q3's collector  | ANSI B | schematic                |
| 4     | The emitter: one capture pin on the ESP32-C6 LCD board | ANSI B | schematic                |
| 5     | Parts list                                             | letter | authored with the sheets |

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D

| REV | DATE       | REVISION                                     | tinymachines               |          |                       |                 | geiger                |
|-----|------------|----------------------------------------------|----------------------------|----------|-----------------------|-----------------|-----------------------|
| C   | 2026-10-05 | the emitter is the ESP32-C6-LCD-1.47, GPIO18 | SHEET TITLE                |          |                       |                 | Cover and sheet index |
| D   | 2026-10-06 | emitter and receiver built and run           |                            |          |                       |                 |                       |
| E   | 2026-10-12 | Q3's collector tap, the box, emitter-0.2     | DRAWING NO.<br>TM-TRNG-001 | REV<br>F | DATE<br>2026-10-13    | SHEET<br>1 of 5 |                       |
| F   | 2026-10-13 | outside the box; both supplies confirmed     | DRAWN BY<br>bisenbek       |          | SOURCE<br>git cf99592 | SCALE<br>NTS    |                       |

D

6

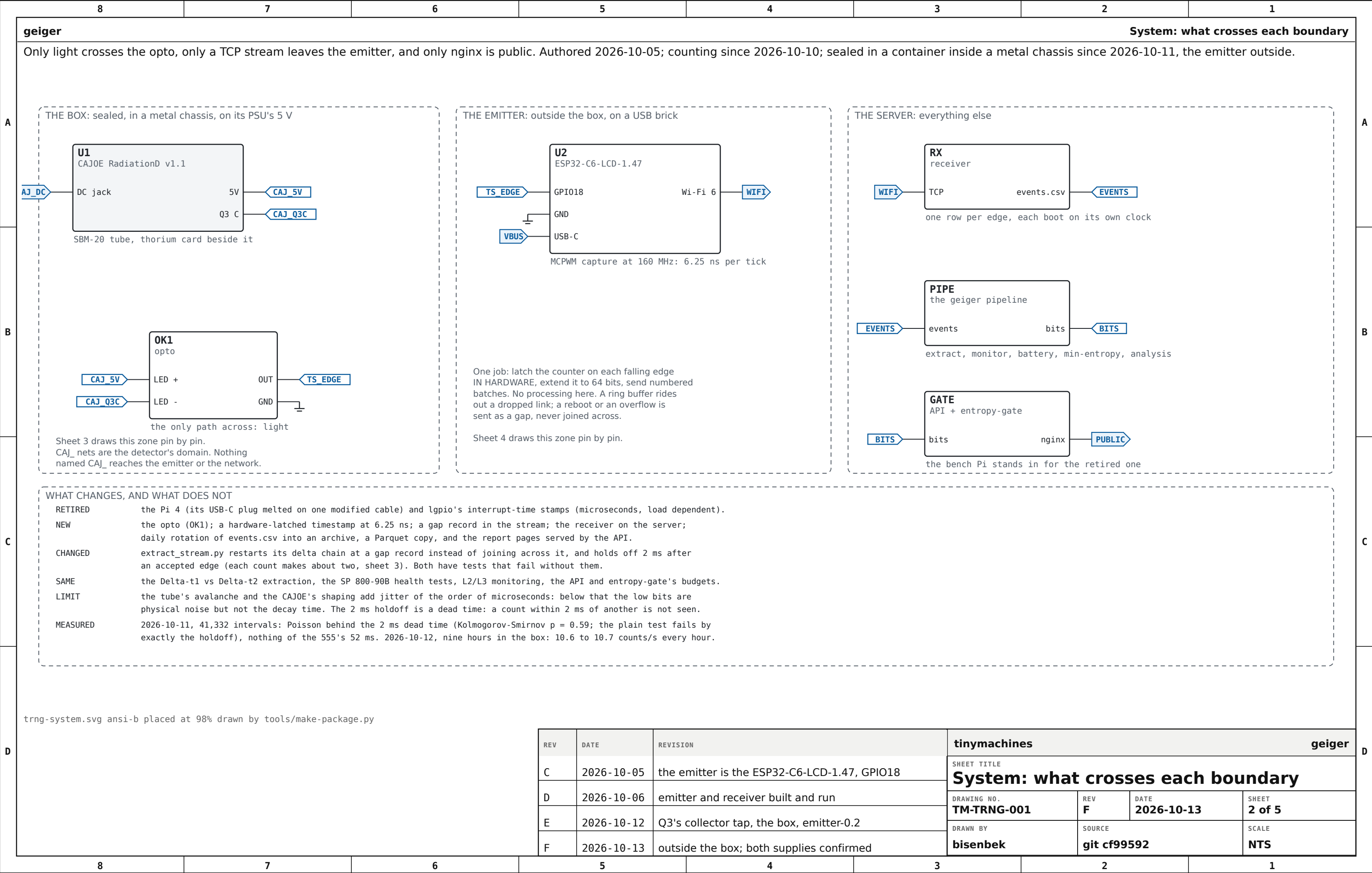
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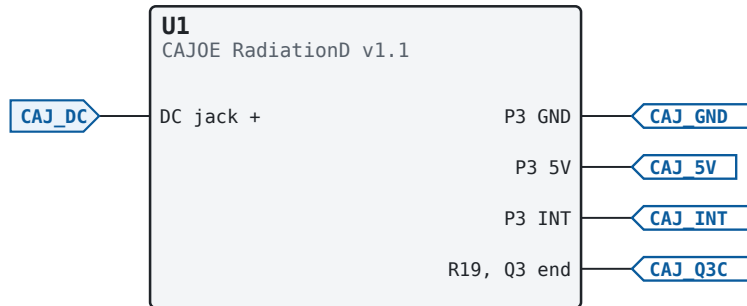


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**The box: the CAJOE on 5 V, the opto on Q3's collector**

Sealed in a heavy-duty outdoor container inside a metal chassis, in a garage out of the sun (since 2026-10-11; a cigar box before that). OK1 is the Iso\_817\_X1 module (a TLP785), the stand-in. Wired 2026-10-10, counting since.

THE DETECTOR'S DOMAIN: the chassis PSU's 5 V line, its own ground



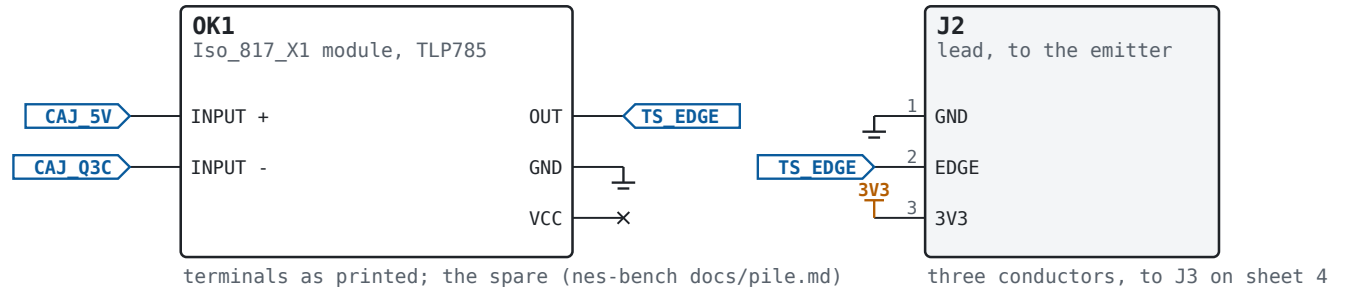
P3 as the v1.1 schematic numbers it: 1 GND, 2 5V, 3 INT. The fourth wire is soldered on.

The DC jack takes a plain 5 V adapter of its own. No cut cables, nothing shared with the emitter: the old bench's modified USB-C lead is what melted.

INT IS NOT AN OPEN COLLECTOR. On the schematic it hangs off Q3's collector through R19 (470k, metered 467k 2026-10-10): it can pass about 5 uA, a thousandth of what an LED needs, which is why 2026-10-06 to 10-08 passed no edge. The scope saw clean 210 us dips there only because it barely loads it.

THE TAP: the end of R19 that does not reach P3 pin 3. That end is Q3's collector, R18's low end and IC2 pin 2. Q3 is the detector transistor; Q4, the other 2N3904, drives the speaker with the 555's 52 ms pulse and is the wrong one. CAJ\_GND and CAJ\_INT go nowhere: the LED loop closes through Q3.

ACROSS THE BARRIER: OK1, and the lead to the emitter



INPUT + on P3 pin 2 (5V), INPUT - or Q3's collector. At idle Q3 is off and its collector sits near 5 V through R18 (47k): nothing flows in the string (the indicator D1, the LED, the module's R1 1k). On a count Q3 pulls the collector to about 0.2 V for the tube's ~210 us and the LED draws about  $(5 - 2.9) / 1k = 2 \text{ mA}$ ; Q3 sinks it. No resistor is added. OUT pulls TS\_EDGE low while the LED is lit; the 4.7k pull-up is at the emitter (R1, sheet 4). The FALLING edge is the timed one.

MEASURED 2026-10-10: each count makes about TWO falling edges, most 150 to 300 us after the first (the slow rise through 4.7k re-crosses the pin's threshold), some under 50 us. The extractor holds off 2 ms; issue 5 is the hardware cure. VCC open: the module's R2 (10k) then pulls nothing.

## THE HOUSING, THE ISOLATION, AND WHAT THE STAND-IN COSTS

|         |                                                                                                                                                                                                                                                                                                                                                                   |
|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| HOUSING | a heavy-duty outdoor container, sealed, inside a metal chassis, in a garage out of the sun (owner, 2026-10-13). The emitter sits OUTSIDE both; the opto lead J2 is the one thing that crosses the two walls. Wi-Fi from outside the metal: -50 dBm (was -69 inside). 10.65 counts/s against 11.5 in the cigar box. The chassis's bond to either ground: not read. |
|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

ISOLATION      only light crosses OK1, and the CAJ\_ nets stop at it, WHILE the CAJOE keeps its own supply and the emitter its own.  
AS BUILT, CONFIRMED 2026-10-13 (owner): the CAJOE on the chassis PSU's 5 V line with nothing else on it; the emitter on a USB power brick. Two supplies, two grounds, one light path. One supply for both would undo this sheet.

STAND-IN      the TLP785's edges take microseconds and move with temperature and LED current: a 6.25 ns stamp mostly measures it.

BUILD a fast logic-output opto with a 3.3 V output side (TLP2361 or HCPL-060L class), not yet ordered; not 6N137 (5 V output side).

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trng-case.svg ansi-b placed at 98% drawn by tools/make-package.py
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